

# Swedish Microwave Days 2023

## D-band LNA in Vertical III-V Nanowire Technology

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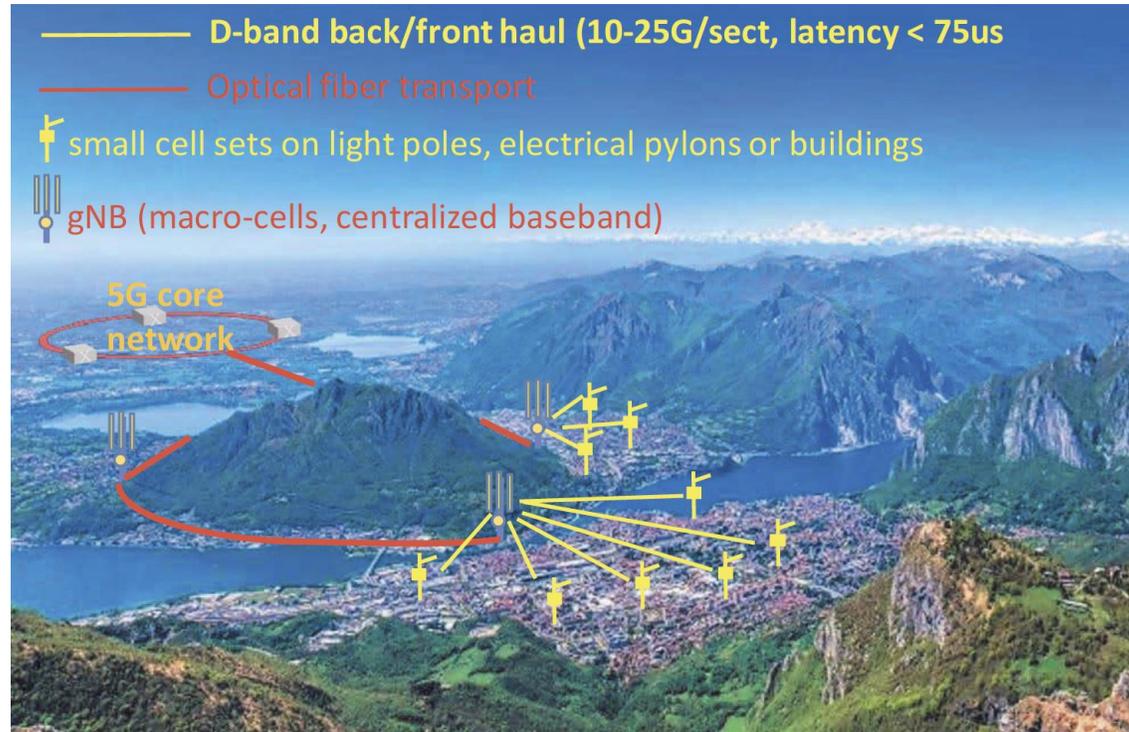


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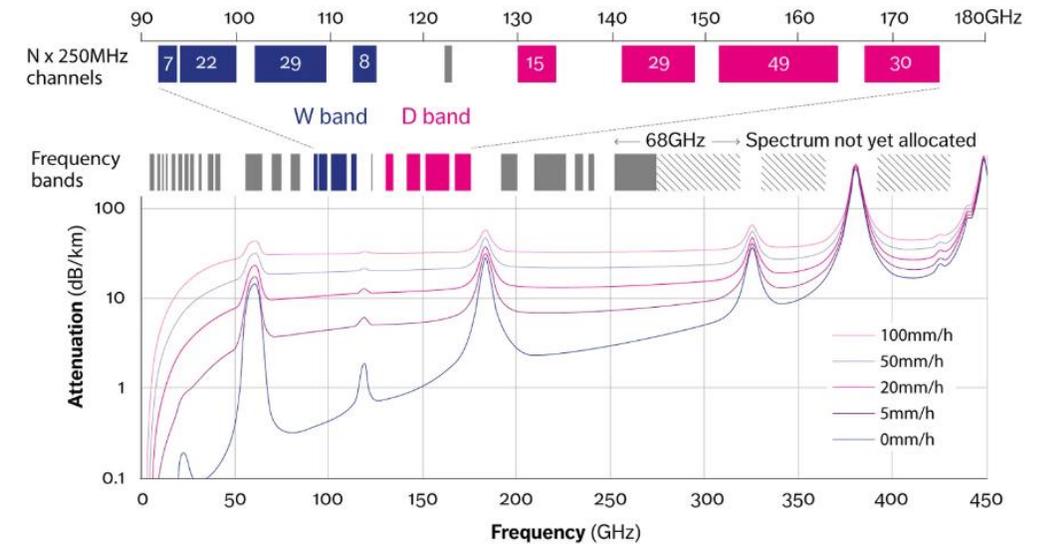


Lomma. Analog & RF Consulting

# Why D-band ?

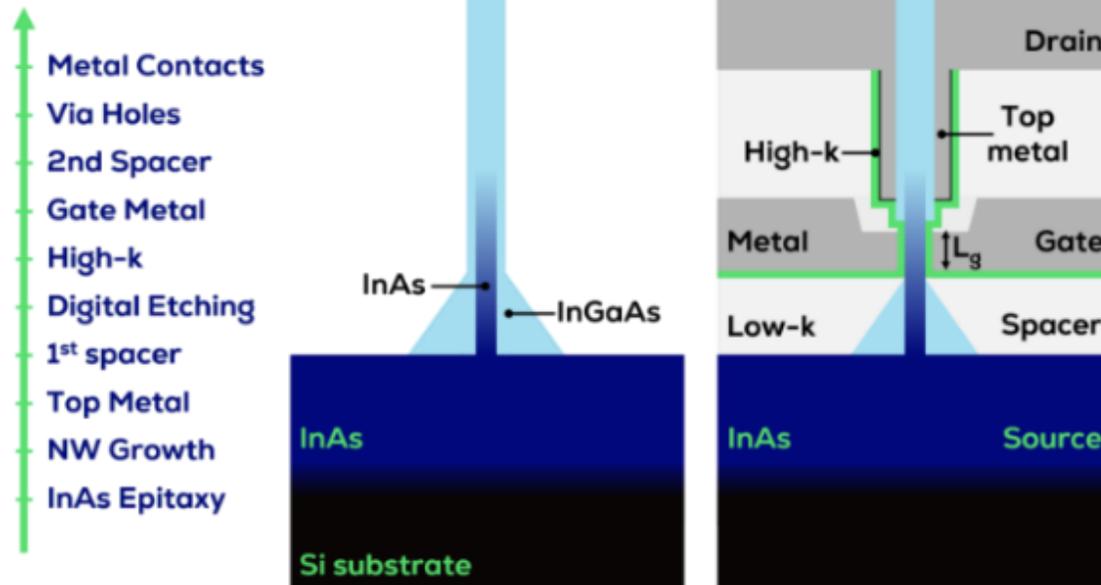


<https://www.h2020-dragon.eu/overview/>



Ericsson review, Microwave backhaul evolution – reaching beyond 100GHz, 2017

# Semiconductor Technology

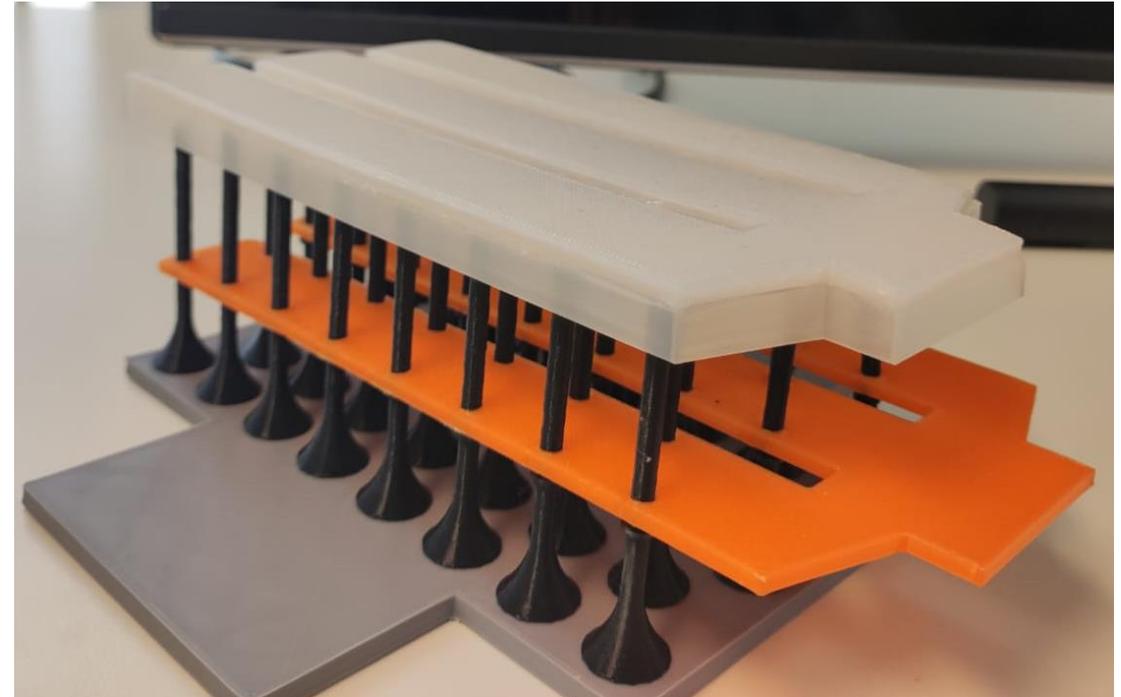


- Vertical structure → low parasitics to substrate
- Simple manufacturing technology
- Higher mobility than Si
- Semi ballistic

# 3D-printed device models



- Single wire device cut in half

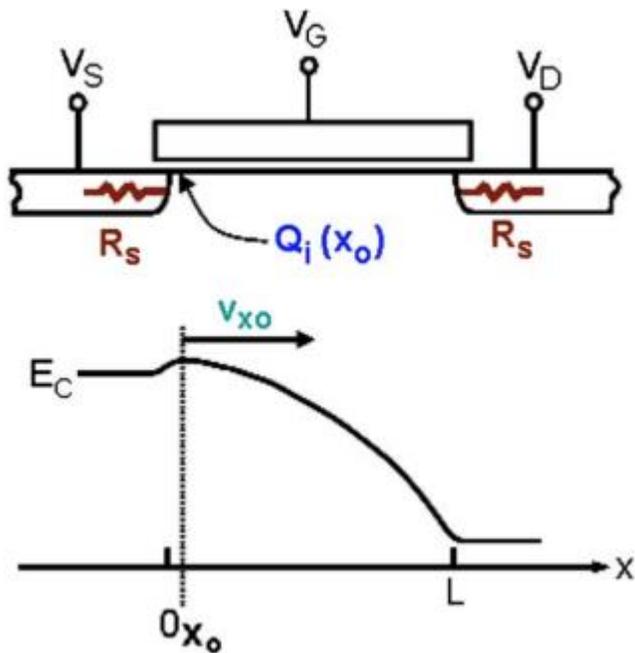


- LNA type device. Input device with:
  - 296 wires in parallel (black)
  - 8 fingers to reduce  $R_g$  (orange)
  - Drain fingers (white) to reduce parasitic capacitance
  - InAs mesa source layer (grey)

# Device model

- **Virtual source model (from MIT)**

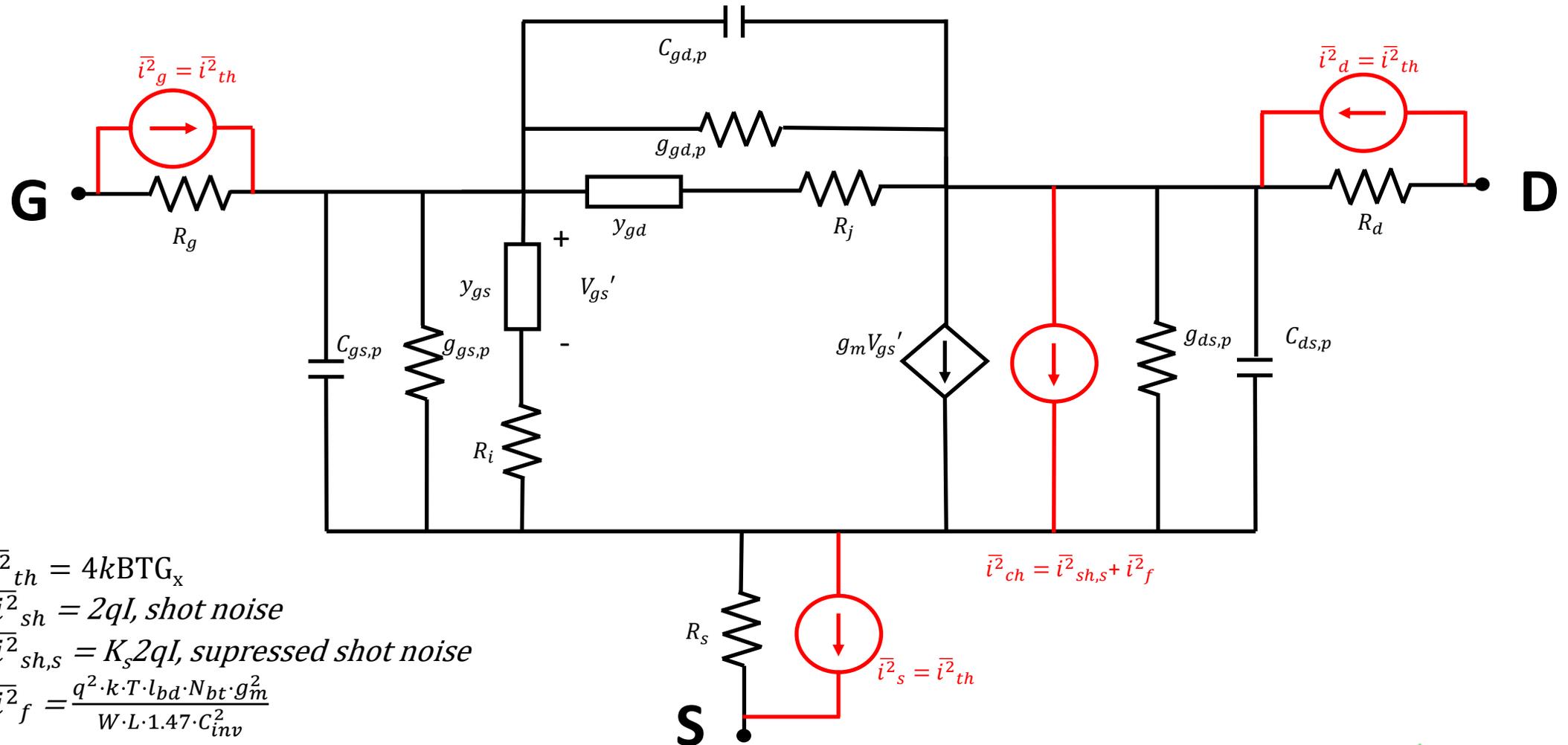
- Semi-empirical model for quasi-ballistic transistors
- Few physical parameters
- Extrapolated from validated devices at  $L_g=120\text{nm}$  with  $f_T/f_{\text{max}}=123/130$  GHz
- This work:  $f_T/f_{\text{max}}=285/418$  GHz for  $L_g=20\text{nm}$



- Virtual-source point  $x_0$ : carrier charge and density defined at this point (at the peak of the conduction band)
- Easiest to calculate charge density at VS point.
- $I_d$ : product of local charge areal density times the local carrier velocity at any point in the channel.
- $I_d = Q_i(x_0) \times v_{x_0} \times (F_{\text{sat}}) \times W$ ,

$$F_{\text{sat}} = \frac{V_{\text{dsi}}/V_{\text{dsat}}}{\left(1 + \left(\frac{V_{\text{dsi}}}{V_{\text{dsat}}}\right)^\beta\right)^{\frac{1}{\beta}}}$$

# Device model with parasitics and noise sources



$$\bar{i}_{th}^2 = 4kBTG_x$$

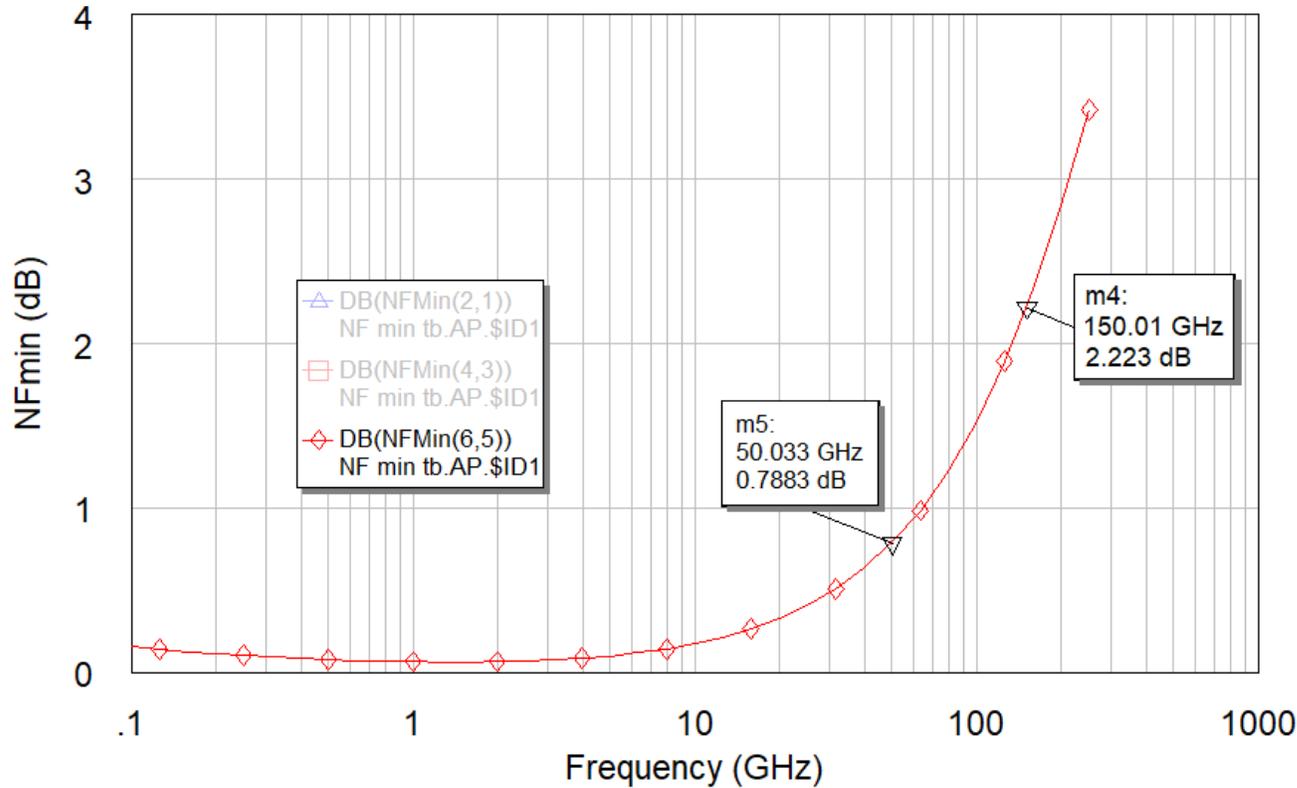
$$\bar{i}_{sh}^2 = 2qI, \text{ shot noise}$$

$$\bar{i}_{sh,s}^2 = K_s 2qI, \text{ suppressed shot noise}$$

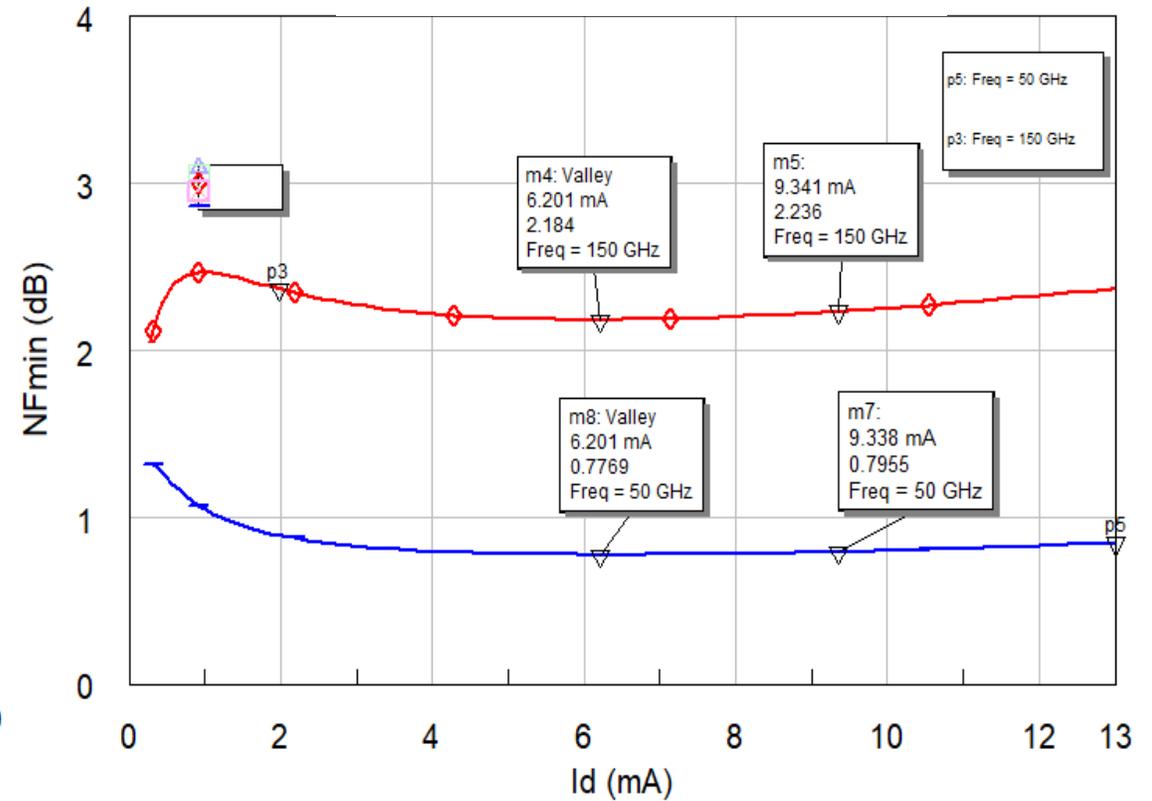
$$\bar{i}_f^2 = \frac{q^2 \cdot k \cdot T \cdot l_{bd} \cdot N_{bt} \cdot g_m^2}{W \cdot L \cdot 1.47 \cdot C_{inv}^2}$$

# Device model-NF<sub>min</sub>

- NF<sub>min</sub> vs frequency for Id=9.3 mA  
(input stage, NW=296, NF=8)



- NF<sub>min</sub> vs I<sub>d</sub> for f=50 and 150 GHz

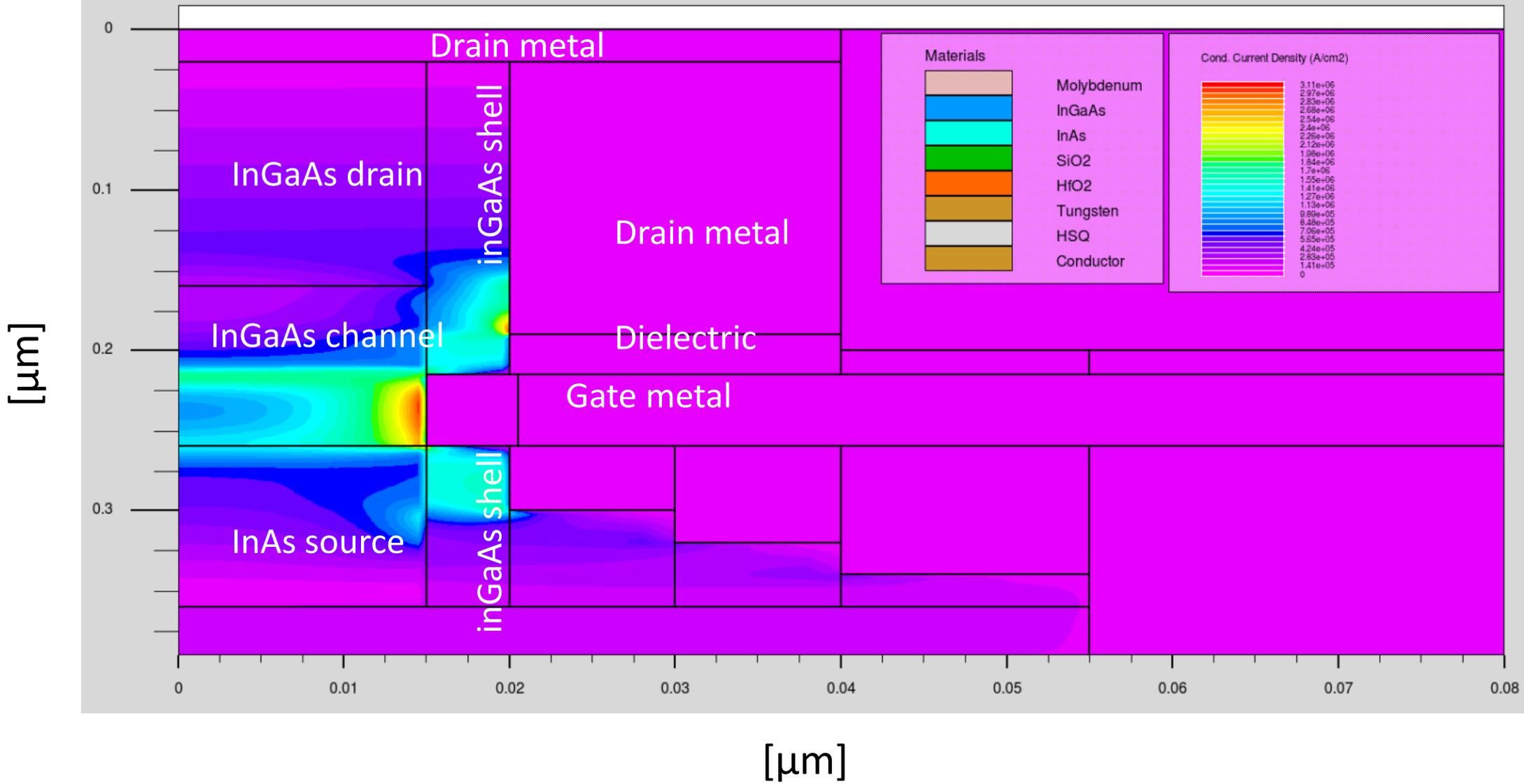


# Technology benchmark-NF<sub>min</sub> @ 50 GHz

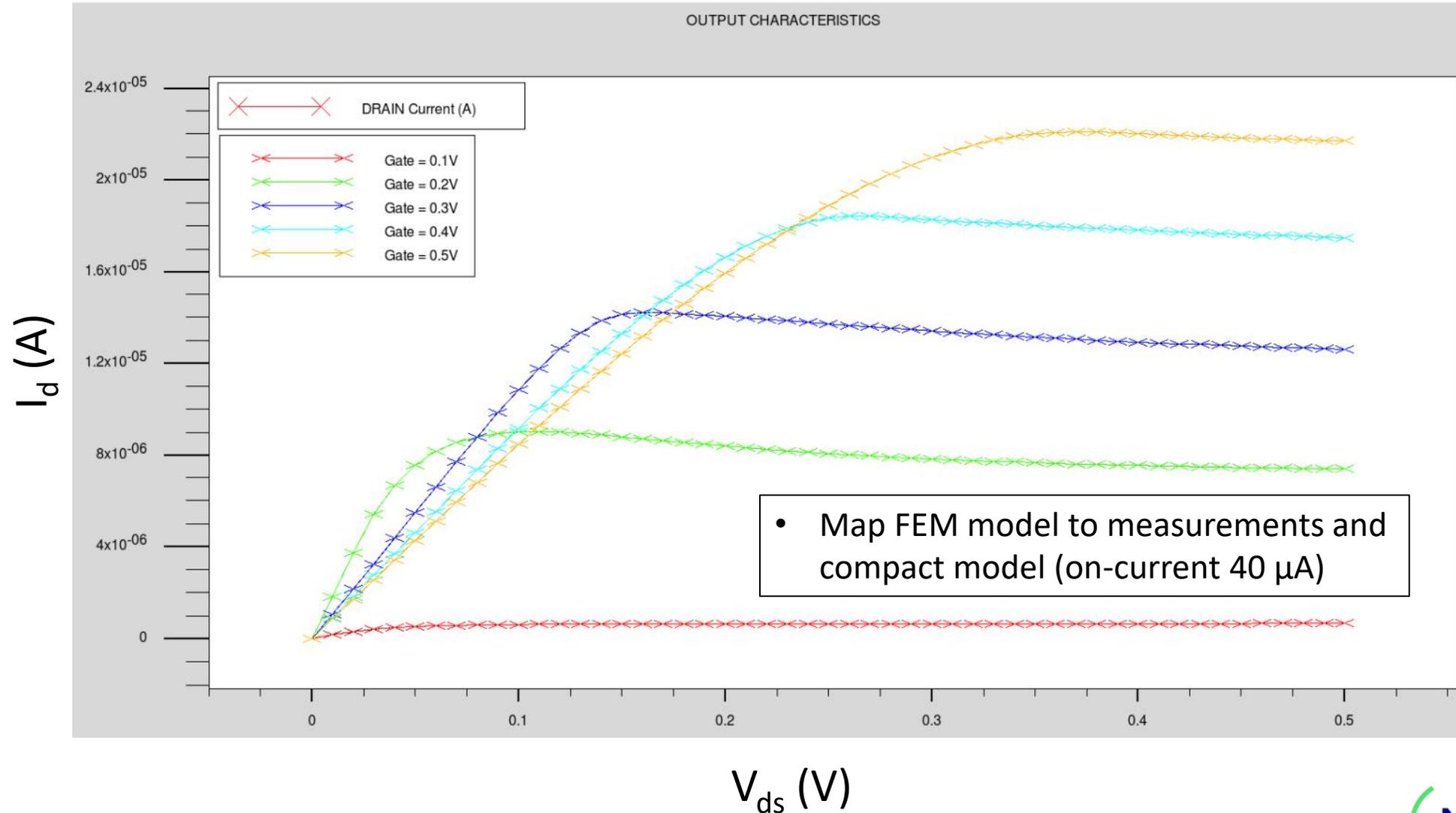
Technology	Feature size (nm)	fMAX (GHz)	Vbr (V)	NFmin (dB) at 50GHz**	Production or research?
GaAs pHEMT	100	185	7	0.5	P
GaAs mHEMT	70	450	3	0.5	R*
GaAs mHEMT	35	900	2	1	R
InP HEMT	130	380	1	<1	R
InP HEMT	30	1200	1	<1	R
GaN HEMT	60	250	20	1	R
GaN HEMT	40	400	42	1.2	R
SOI CMOS	45	280	1	2-3	P
SiGe-HBT	130	400	1.4	2	P
InP DHBT	250	650	4	3	R*
InP DHBT	130	1100	3		R
<b>NordAmps</b>	<b>20</b>	<b>418</b>	<b>0.6</b>	<b>0.8</b>	<b>R</b>

# Rotational symmetric FEM structure: Current density

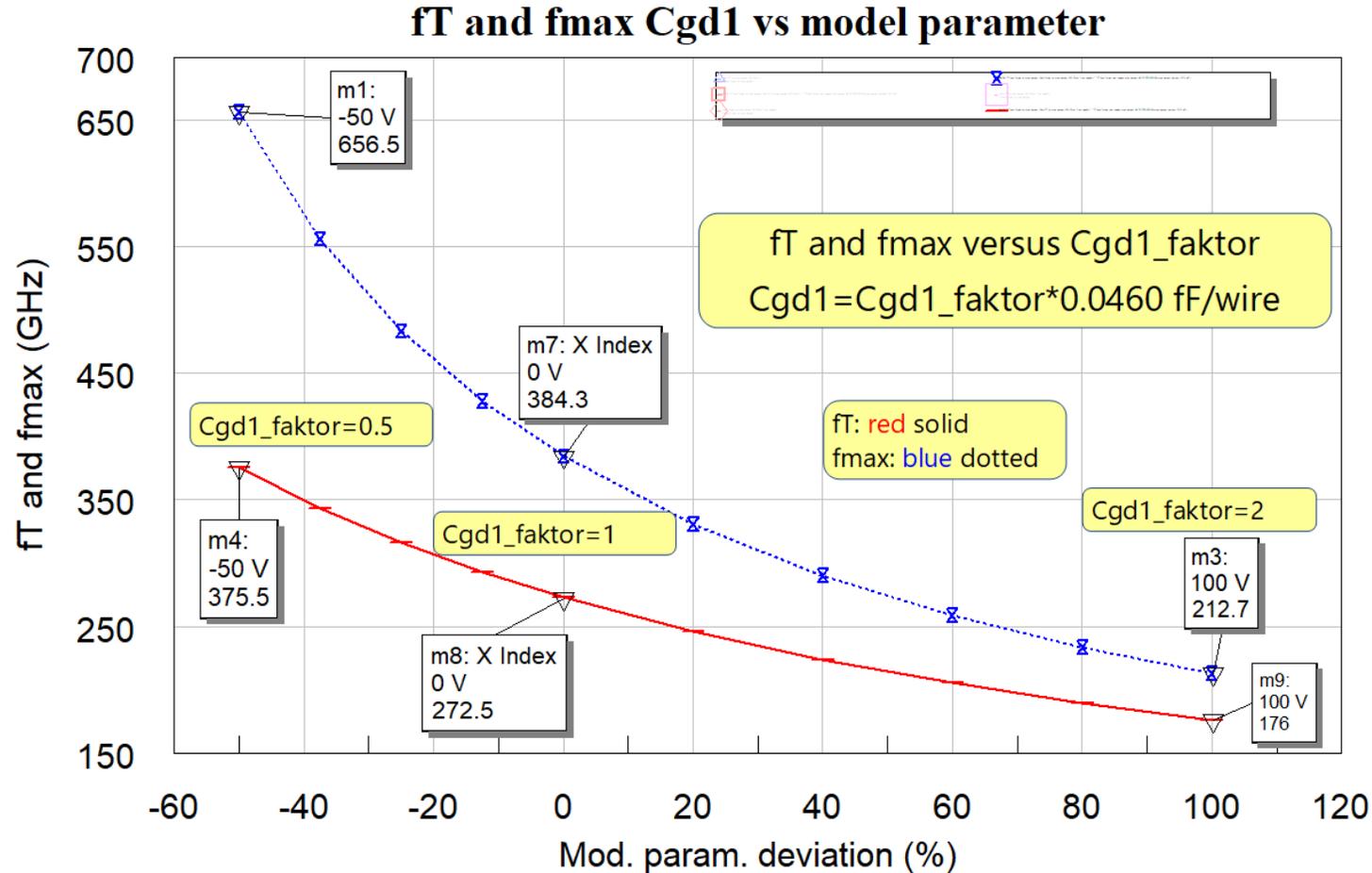
CURRENT DISTRIBUTION  
Applied potential Gate=0.3V Drain=0.5V



# FEM: Silvaco Blaze output characteristics



# Device optimization with VerilogA compact model



- **Starting point:**  
 NW=300 wires  
 NF=6 fingers  
 $L_g=25\text{nm}$   
 →  
 **$f_T = 272$  GHz and  $f_{max} = 384$  GHz**
- Simulate sensitivity in maximum  $f_T/f_{max}$  vs  $I_d$  for 11 model parameters
- Highest sens. for  $C_{gd}$

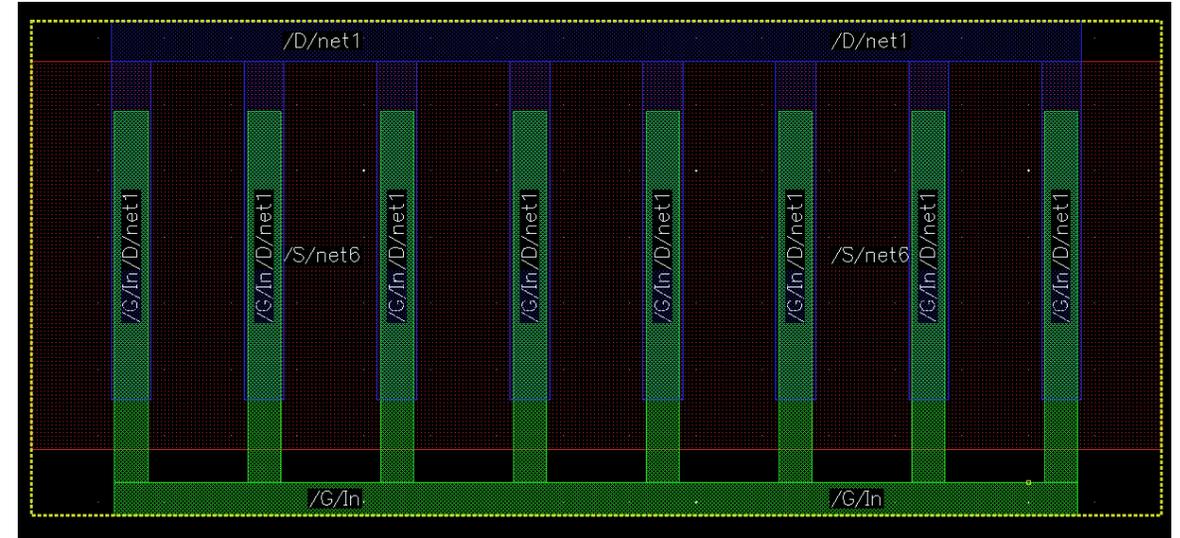
→ Process optimization

# Process Design Kit (PDK)

- **PDK in Cadence**

- VerilogA model code
- Parasitic extraction in Quantus
- Electromagnetic simulations in EMX
- Fast convergence, both in Periodic Steady State and Harmonic Balance

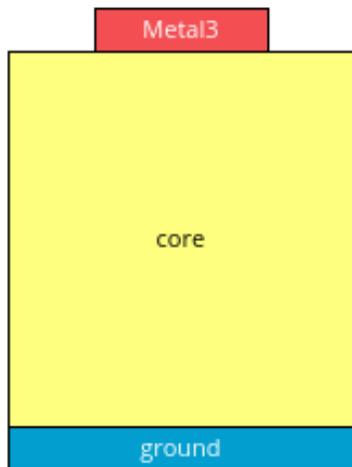
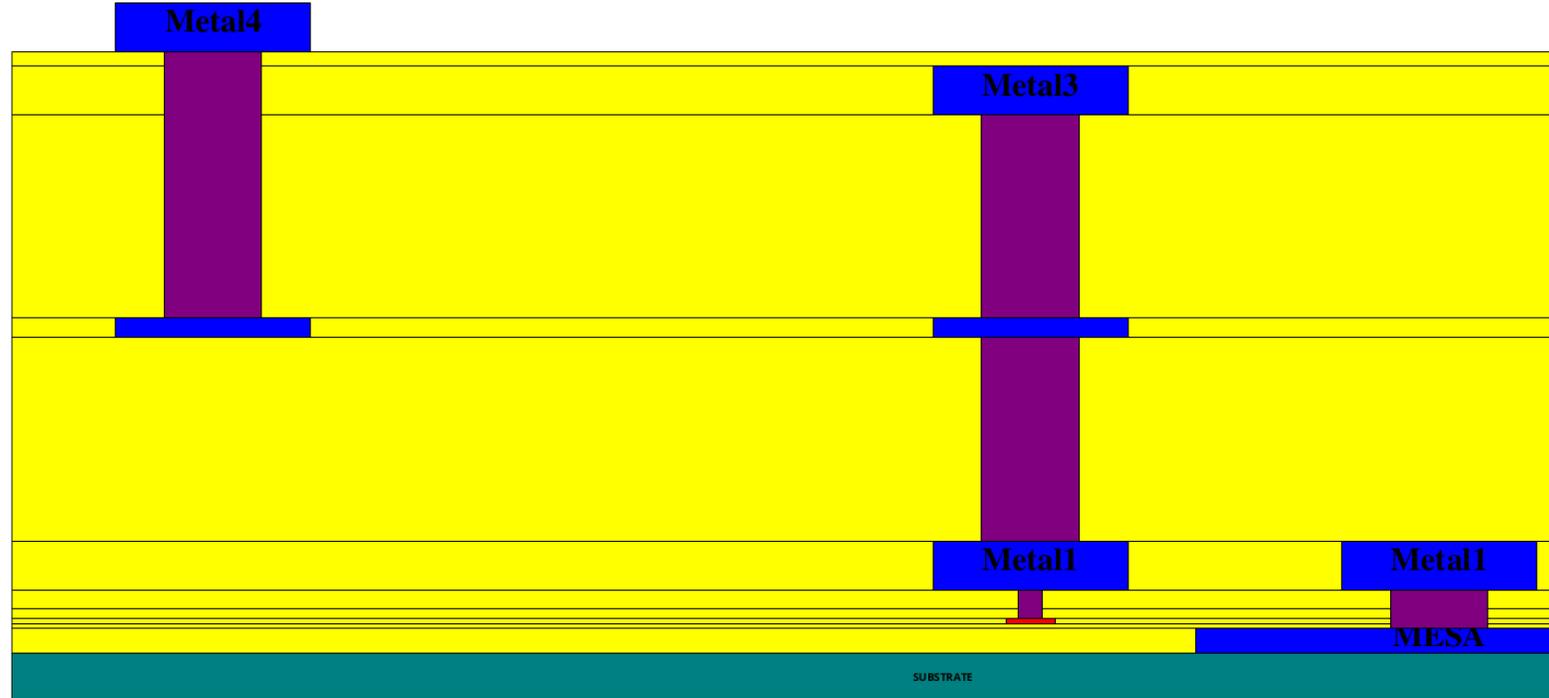
- Model code also for Microwave Office (AWR)



- **Scalable P-cells**

- N-type transistor
- MIM- capacitors: 15 and 200nm dielectrics
- Thin Film Resistor (TFR):  $50 \Omega/\square$
- Transmission lines
- Inductors

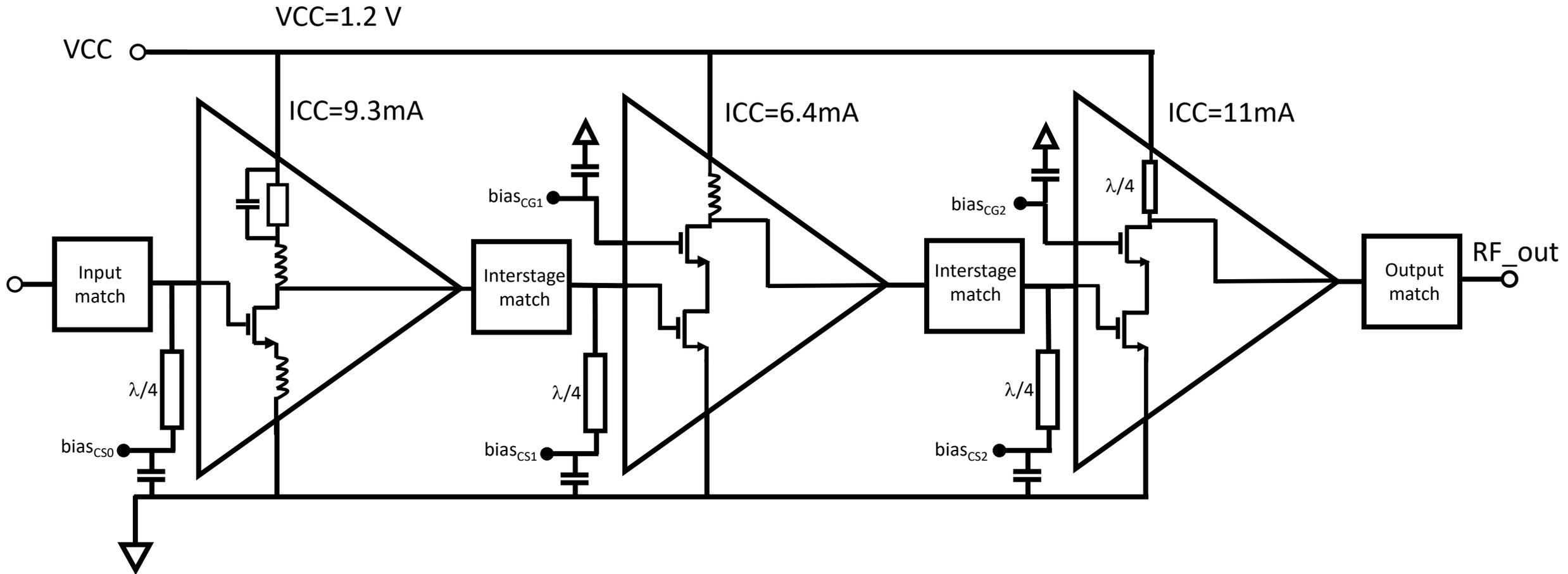
# Back End of Line (BEOL)



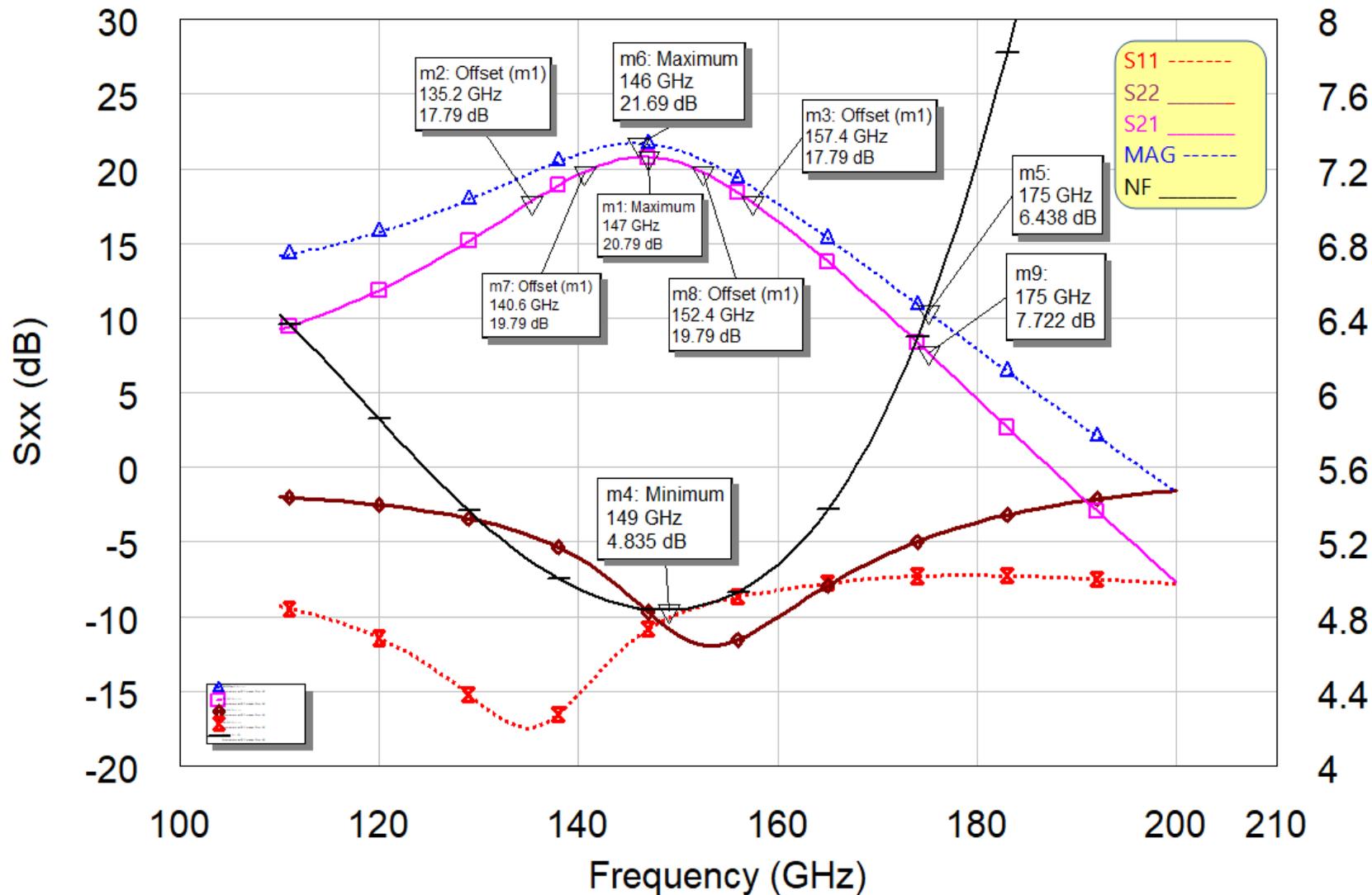
Type	Layer Name	Thickness	Material
Conductor	Metal3	0.5e-6	mCond1
Dielectric	core	4.2e-6	mDiel1
Reference	ground	0.5e-6	mCond1

- 0.5 $\mu\text{m}$  Au with BCB dielectric  $\epsilon_r=2.65$
- 4.2  $\mu\text{m}$  to ground plane

# 3-stage LNA design



# Simulation results 3-stage LNA



- $S_{21}=20.8$  dB@147 GHz
- $NF=4.8$  dB@149 GHz
- Broadband  $S_{11}$

- Low gain @ 175 GHz
-  NF increase

- **Compression point and linearity:**  
 $ICP_{1dB}=-21$  dBm @ 146 GHz  
 $IIP_3=-11$  dBm for two tones @146 and 147 GHz.

# Conclusions

## D-band LNA in Vertical III-V Nanowire Technology

- Compact model + Cadence PDK
- Predictive modeling → close to commercial NF performance @ lower D-band frequencies
- III-V technology with  $f_T/f_{\max} = f_T/f_{\max} = 285/418$  GHz
- Minimum NF=4.8 dB @ 149 GHz
- Further process optimization → Increased competitiveness

An interesting technology for  
future millimeter wave  
applications !